

FIG. 1



| | | | | | | | | | | | | | | | | |
|--------|-----------|----|--------|---|--------|---|-------|---|-----|----------|--------|----------|--------|------|----------|--|
| | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | | |
| Word 0 | Rx_DV = 0 | | Rx_Cyc | | Tx_Cyc | | Mdout | | 00 | PtM_mode | Even | Rx_Er | | | | |
| Word 1 | | | | | | | | | 01 | RST_RQST | SQL | | Duplex | Seed | I_Er | |
| Word 2 | | | | | | | | | 10 | rsrsvd | rsrsvd | | rsrsvd | Link | Int_rqst | |
| | | | | | | | | | CRS | | | Duplex | | | | |
| | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | Seed | | | | |
| | | | | | | | | | | | | Link | | | | |
| | | | | | | | | | | | | Int_rqst | | | | |

FIG. 2



| | |
|----|------------|
| 11 | Rx_Dv = 1 |
| 10 | Rx_Cyc = 1 |
| 9 | Tx_Cyc |
| 8 | Rdata0 |
| 7 | Rdata1 |
| 6 | Rdata2 |
| 5 | Rdata3 |
| 4 | Rdata4 |
| 3 | CRS |
| 2 | Rdata5 |
| 1 | Rdata6 |
| 0 | Rdata7 |

FIG. 3



| | |
|----|------------|
| 11 | Rx_Dv = 1 |
| 10 | Rx_Cyc = 1 |
| 9 | Mdout |
| 8 | Rdata0 |
| 7 | Rdata1 |
| 6 | Rdata2 |
| 5 | Rdata3 |
| 4 | Rdata4 |
| 3 | CRS |
| 2 | Rdata5 |
| 1 | Rdata6 |
| 0 | Rdata7 |

FIG. 4



| | |
|----|------------|
| 11 | Rx_Dv = 1 |
| 10 | Rx_Cyc = 0 |
| 9 | Tx_Cyc |
| 8 | Mdout |
| 7 | rsrvd |
| 6 | rsrvd |
| 5 | rsrvd |
| 4 | rsrvd |
| 3 | CRS |
| 2 | rsrvd |
| 1 | rsrvd |
| 0 | rsrvd |

FIG. 5

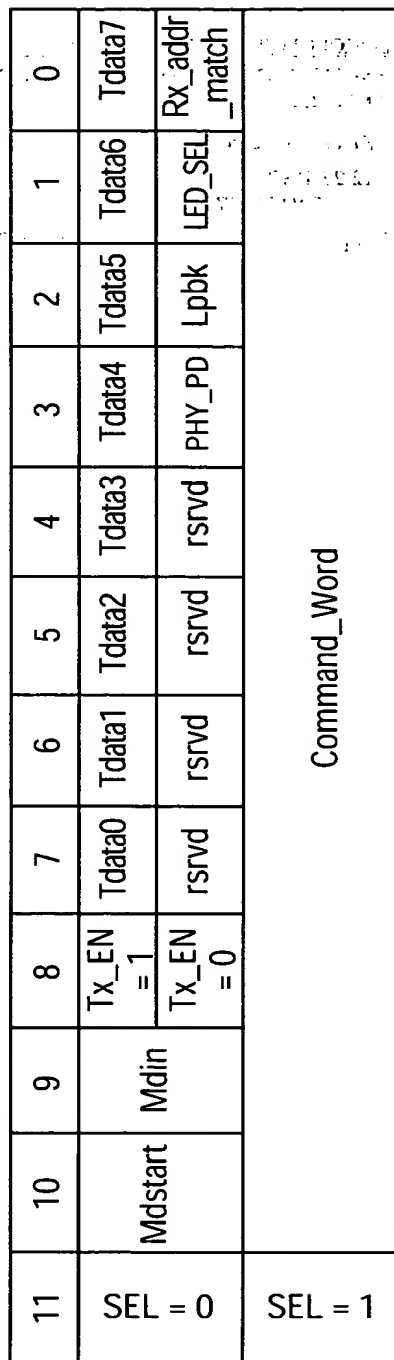


FIG. 6



| | | | | | |
|-------|---------|----|----|-----------------------|-------------------|
| Mdin | IDLE | ST | OP | Reg Addr (10 bits) | Data (16 bits) |
| | 000...0 | 1 | 01 | | |
| Mdout | IDLE | | | | |

FIG. 7



| | | | | | | |
|-------|---------|----|----|-----------------------|--------------|-------------------|
| Mdin | IDLE | ST | OP | Reg Addr (10 bits) | Wait Time | IDLE |
| | 000...0 | 1 | 10 | | 0001 | 000...0 |
| Mdout | IDLE | | | | 0001 | Data (16 bits) |

FIG. 8

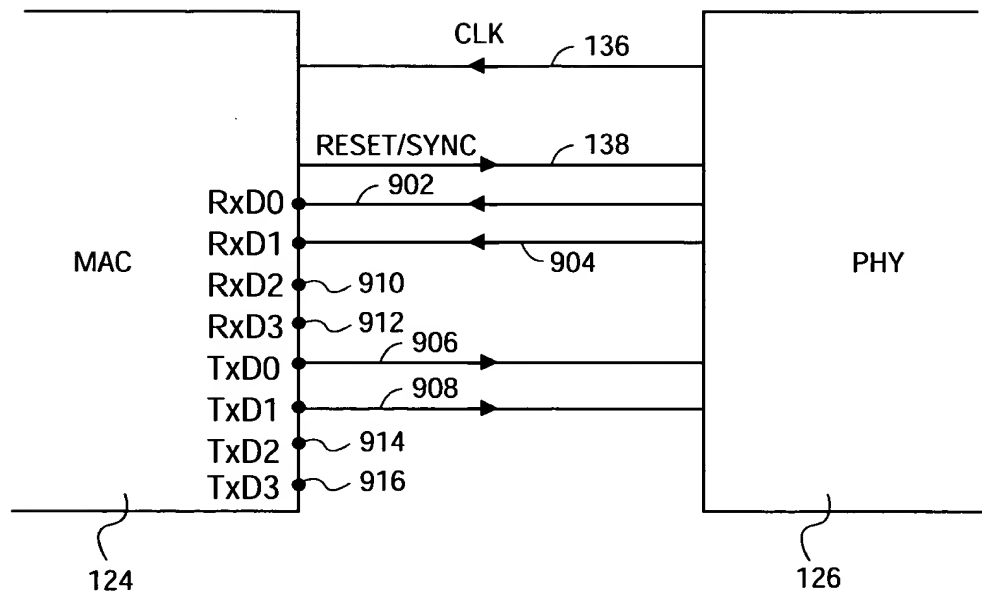


FIG. 9

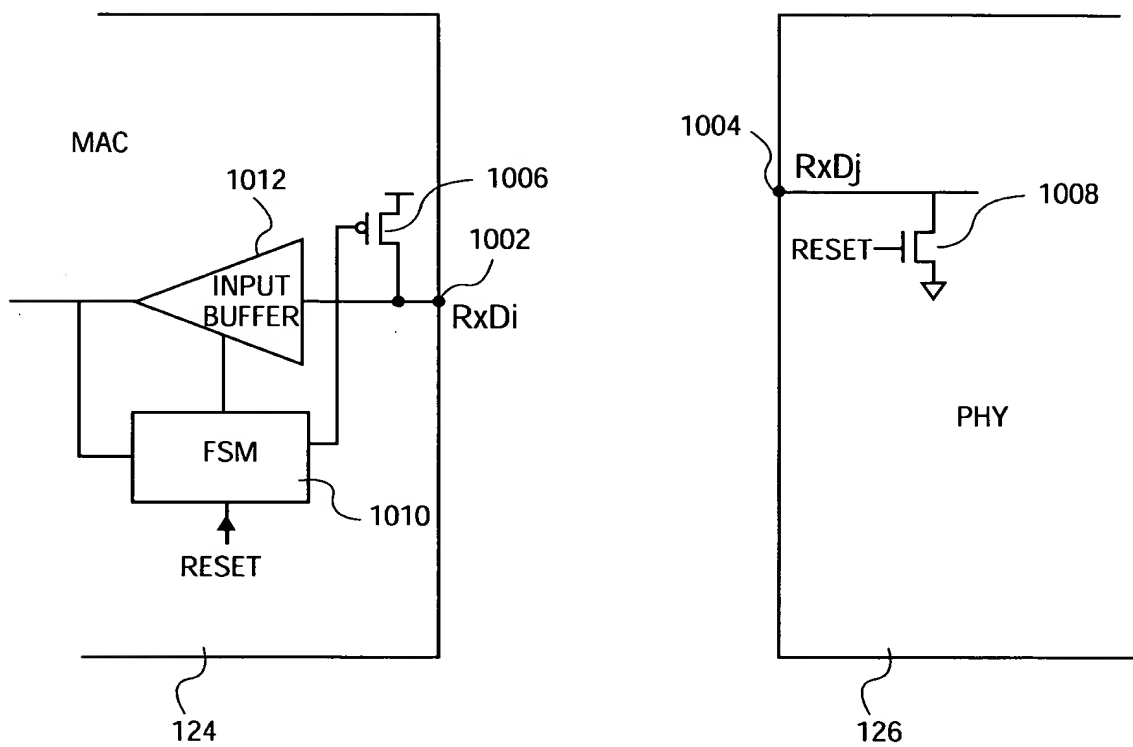


FIG. 10

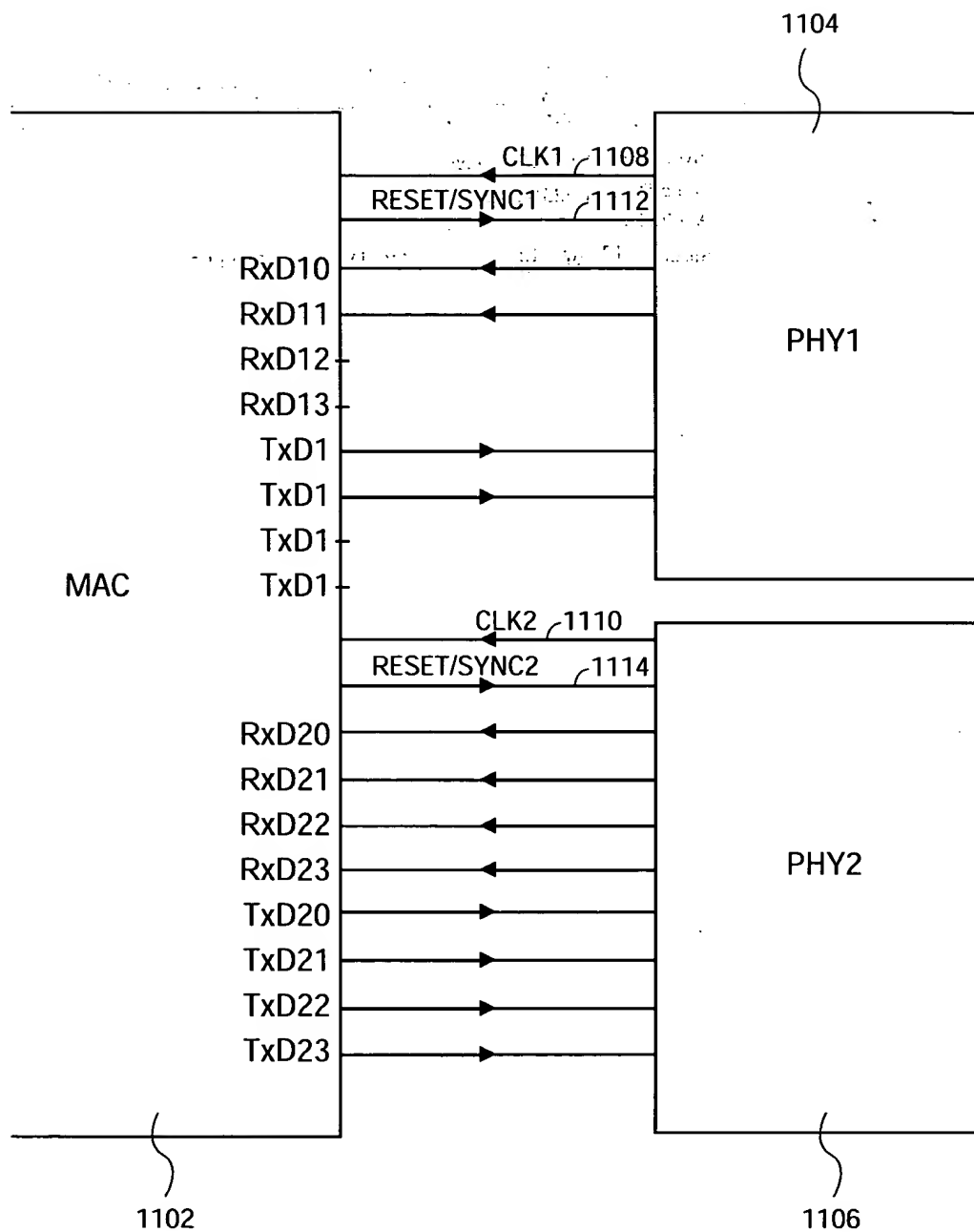


FIG. 11

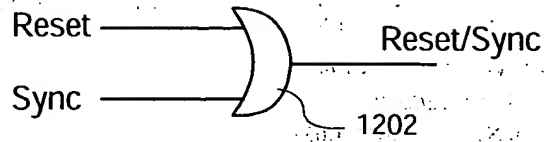


FIG. 12A

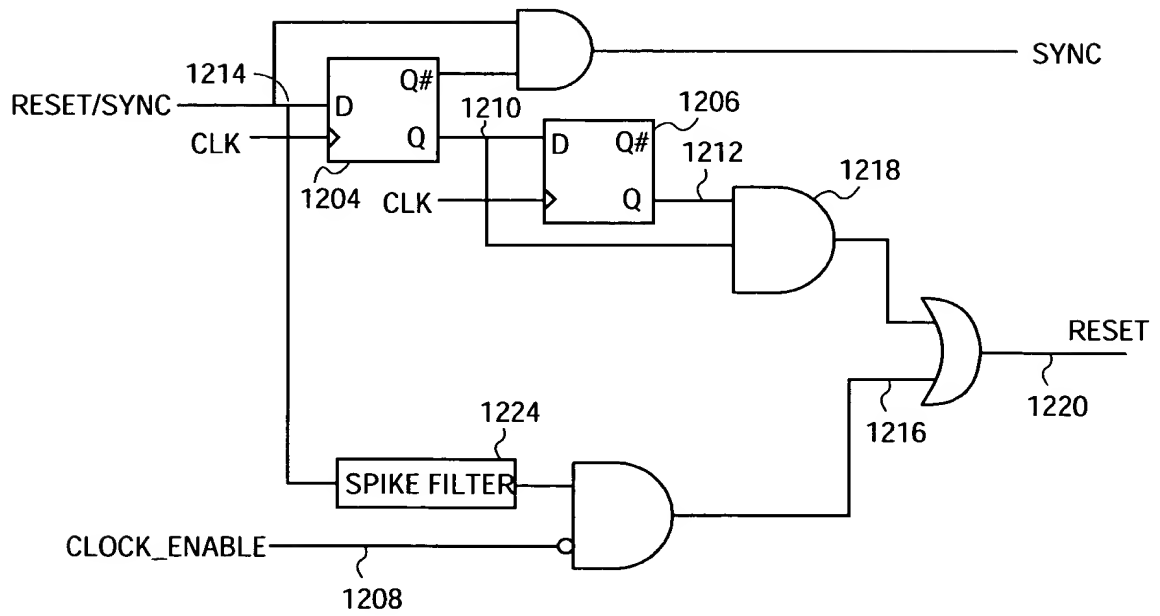


FIG. 12B